

COPPER METALLIZATION OF SEMICONDUCTOR INTERCONNECTS – -- ISSUES AND PROSPECTS

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The copper electroplating process for ‘dual damascene’ metallization of semiconductor interconnects is critically reviewed and the breakthroughs that made this process possible are examined. Special emphasis is placed on analyzing the critical issues, barriers, and future prospects for this technology. The parameters that control the deposit thickness distribution on the macroscopic (wafer) scale and on the microscopic (via) scale are compared. Effects due to the resistive seed layer and mass transport limitations, particularly on the micro-scale, are analyzed. Preferred electrolyte compositions, including the effects of plating additives are discussed. Issues pertaining to cell design, scaling and preferred process conditions are considered.

Electroplating applications in microelectronics have been traditionally limited, with a few exceptions, to the metallization of printed wiring boards, contacts, and chip carriers, and to the fabrication of magnetic storage devices. Chip level metallization and particularly the extensive interconnect network that carries signals between the individual transistors have been fabricated exclusively of aluminum or aluminum-copper alloys using vapor-phase (‘dry’) techniques. This situation has been undergoing a remarkable change in the past two years following IBM’s striking announcement [1,2] of their commitment to replace the conventional vapor deposited aluminum by electroplated copper. This paradigm shift has now been incorporated into Sematech’s road map [3] and is being integrated, worldwide, into production. The commercial implementation of the plating process in an industry that has been skeptical of wet processing is quite remarkable.

RATIONALE AND ADVANTAGES OF COPPER METALLIZATION

The direct impetus for the shift from aluminum to copper has been the ever-shrinking device dimensions that contribute to a decreasing gate (transistor) delay, however, the increased resistance of the correspondingly thinner interconnects brings about a much longer interconnect time delay. Assuming that the interconnect is a metallized via of radius ‘r’ as shown schematically in Fig. 1, we find that its electrical resistance is proportional to its length ‘l’ and inversely proportional to its cross-sectional area:

$$R = \rho l / \pi r^2 \quad [1]$$

The corresponding interconnect time delay is:

$$\tau = RC = C \rho l / \pi r^2 \quad [2]$$

Clearly, as the radius (which is proportional to the line width) decreases, the interconnect time delay increases.

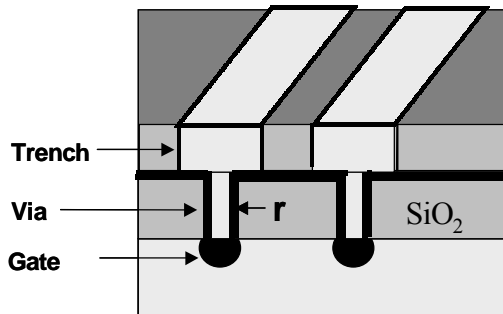


Fig. 1: A schematic cross-section showing a trench and a via interconnect structure. As the via becomes narrower, the resistance increases.

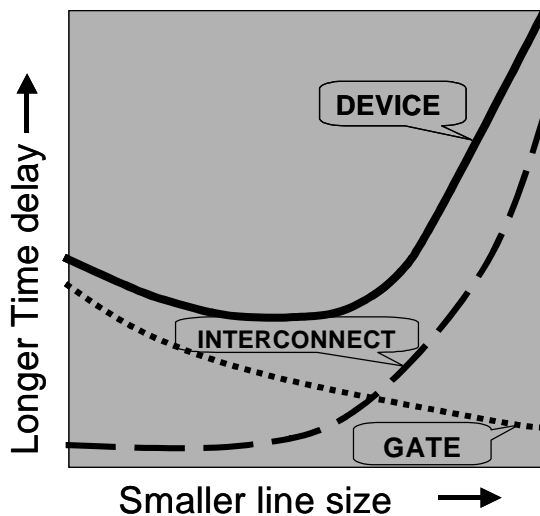


Fig. 2: A schematic representation of the time delays in a device. The overall time delay (top curve) is due to contributions from both the gate (decreasing with smaller line width) and the interconnect (which increases as line width shrinks). Present line width (0.18 μm) corresponds approximately to the minimum in the overall delay. Next generation of 0.13 μm , unless converted to copper, will already be within the steep ascent on the right.

As shown schematically in Fig. 2, the overall time delay of the device, which consists of the sum of the time delays of the interconnect and the gate, increases sharply at small line widths. Unless the resistivity, ρ , (and/or the capacitance, C , which is proportional to the dielectric constant) is decreased, the next generation of microprocessors, with line width of 0.13 μm , will experience an unacceptable increase in the overall time delay. The bulk resistivity of aluminum is 2.65 $\mu\Omega\text{cm}$. Only two metals offer a lower resistivity: copper (1.68 $\mu\Omega\text{cm}$), and silver (1.59 $\mu\Omega\text{cm}$). Concerns over the electromigration of silver rule it out, and copper has been selected as metallization medium with an expected reduction of the time delay by about 40%. In parallel, a new, lower dielectric medium is sought to replace the SiO_2 ($K \sim 4$). Material candidates include various organic compounds, carbons, and aerogels. These materials are typically brittle and their ability to withstand conventional CMP is questionable.

The higher conductivity of copper not only reduces the delay time but it also enables higher current densities at lower voltages, minimizing heat generation and power requirements. Additionally, the use of copper enables better scaling of the interconnect hierarchy, providing for thinner lines at the lower levels where the current density is lower.

Copper cannot be effectively applied by ‘dry’ deposition techniques: PVD does not provide acceptable fill and CVD of copper requires costly, unstable and hazardous organo-metallics. Of the ‘wet’ processes, electroplating has been selected as the process of choice since electroless plating is slower, involves more complex and costly chemistry and controls, and the bath requires frequent replacement. Moreover, electroplating is characterized by a faster deposition rate ($\sim 1 \mu\text{m}/\text{min}$) than electroless plating ($\sim 0.2 \mu\text{m}/\text{min}$), CVD ($\sim 0.2 \mu\text{m}/\text{min}$) or PVD ($0.05\sim 0.1 \mu\text{m}/\text{min}$), and requires less costly equipment than the vacuum based processes.

A major advantage of electroplating is that it enables a more efficient processing sequence, the so-called ‘dual damascene’ process that is shown schematically in Fig. 3. Since both the trenches and the vias are metallized in a single electroplating step, the number of process steps is cut to about one half, resulting in lower cost, less equipment and space requirements, and potentially fewer defects.

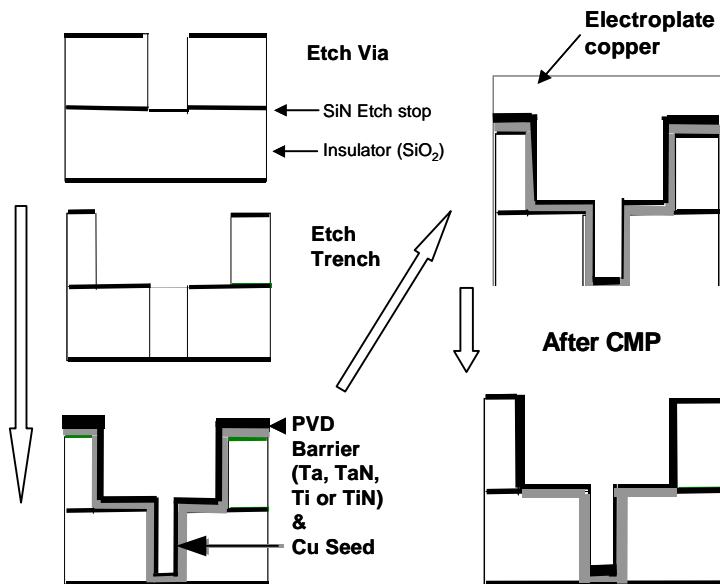


Fig. 3: Steps in the dual damascene process. The trenches and the vias are both metallized in a single plating step. The plating generates an ‘overburden’ of copper which is removed by CMP. The illustrated process steps are repeated to form all interconnect layers. Not shown are the preceding dielectric deposition and the lithography steps, the CVD deposition of the barrier layer (TaN or TiN), the PVD deposition of the copper seed layer and the annealing step of the plated copper that is commonly applied prior to CMP.

An additional, highly important, advantage of the copper interconnects is that they offer a much better electromigration stability than aluminum or copper-aluminum alloys, thus enabling a higher current density and sustaining the trend for narrower line width at a lower failure rate. Data by IBM [4] and Motorola [5] researchers indicate that time-to-failure of copper interconnects exceed that of aluminum and aluminum-copper alloys by a factor of about 10 to 100. Preliminary observations suggest that trace amounts of

carbon (and possibly other elements), which incorporate within the copper during plating, further contribute to electromigration stability.

PLATING PROCESS REQUIREMENTS

The requirements imposed on the copper metallization process are quite severe. An extremely uniform (less than 2-3% thickness variation across the wafer) copper layer must be plated with excellent gap-fill properties onto a thin (500-2000Å), quite resistive copper seed through contacts along the circumference of the wafer. Due to the scarcity of wafer area, only a small region may be expended for contact purposes, and the deposit uniformity must extend to the wafer circumference, with only a few mm edge exclusion. The plated copper must adhere well to withstand subsequent CMP, including the edge regions. Defect-free fill of dual damascene structures with 10:1 aspect ratios and diameters down to 0.1 μm, sharp edges and vertical (or occasionally, re-entrant) sidewalls must be routinely achieved, often with only a marginal seed layer. Extreme properties requirements are imposed on the plated copper. These include electromigration performance, conductivity, mechanical properties (e.g., stress), grain size (larger preferred), reflectivity, and chemical purity (although earlier specifications for extreme purity have been relaxed, recognizing the potential benefit of trace elements on electromigration). The plating process must be fast (>50 wafers/hr/plating cell), robust, and exhibit long-term stability.

KEY ISSUES IN COPPER METALLIZATION OF INTERCONNECTS

In addition to the cultural issue of extending a 'classical' technology that is occasionally viewed as highly empirical into the forefront of semiconductor processing, the process requirements pose a number of critical technological barriers that had to be overcome:

(a) Bottom-up fill of micro-scale features - The most critical barrier to copper metallization by plating has been the requirement to completely fill-up the vias and trenches by copper, assuring that no trace electrolyte is trapped. To achieve this, copper may not be plated in its 'normal' mode where the top ridges build-up first in a dog-bone fashion (due to enhanced transport and a higher field at the small curvature, highly accessible rims), generating a trapped void [Fig. 4 (a)]. Nor is it acceptable to plate conformally (by suppressing the deposition process through the use of excess additives) as shown schematically in Fig. 4 (b). The seam that is formed at the center may interfere with the copper recrystallization and may still trap some electrolyte. Clearly, the preferred process is that depicted in Fig. 4 (c), where the copper growth starts at the bottom of the via and rapidly progresses upwards. Since not only the bottom but also the top and sidewalls of the via are metallized by copper seed, and since the plating of the via emanates from its top (highest transport and field), it is not easy to achieve this 'unnatural' 'bottom-up' fill.

The key has been IBM's discovery that the bottom-up fill can be achieved through the use of a special mix of plating additives that by differential adsorption on the flat surface and within the via can affect the 'bottom-up' fill (Fig. 5). The additives mix typically contains a relatively large, slow diffusing, suppressing additive (e.g.

polyethylene glycol) that preferentially adsorbs on the flat surface and the rim of the vias and slows down the deposition at those locations, in combination with another additive (e.g. an organic sulfur compound) that preferentially adsorbs within the via and enhances rapid deposition (or negates the effects of the suppressing additive) at its bottom.

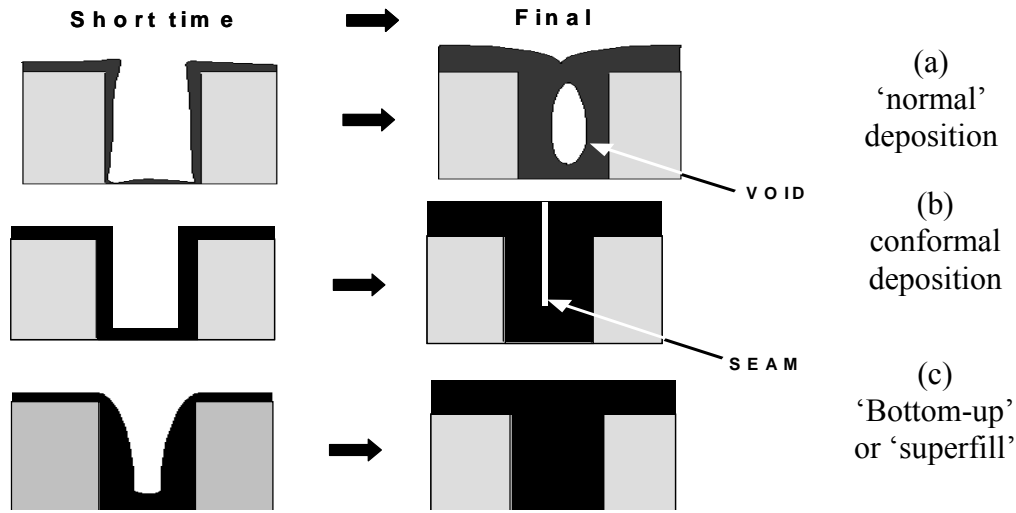


Fig. 4: Via fill patterns. (a) 'Normal' deposition leads to 'dog-boning' and eventually to a trapped void due to the preferential accessibility of the rim. (b) Conformal deposition in the presence of excess suppressing additives leads to an unacceptable seam at the center. (c) Desired 'Bottom-up' or 'superfill'.

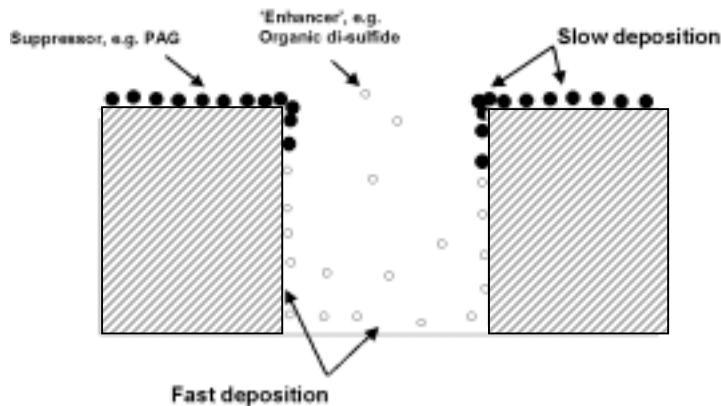


Fig. 5: Additives distribution near and within a via. Variable adsorption leads to variable kinetics and to bottom-up fill. Large, slow diffusing, deposition suppressor adsorbs primarily at the flat surface and along the rim, while a fast diffusing, smaller additive, penetrates the via and enhances the deposition rate there.

Fig. 6 shows cross-sections through plated trenches exhibiting the characteristics shown in Fig. 4.

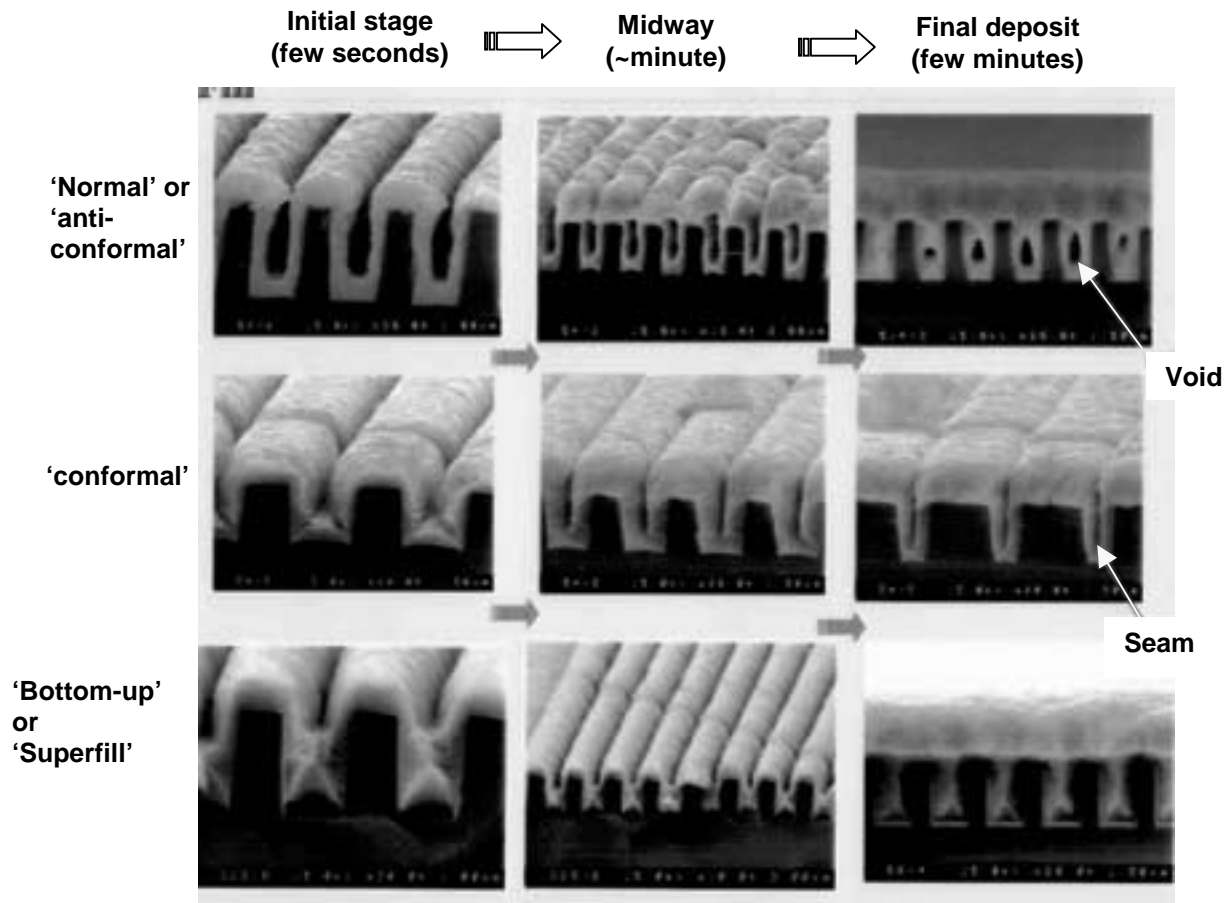


Fig. 6: Time evolution in trench fill. *Top row*: ‘normal’ deposition without proper additives and at excessive current density. A trapped void is noted at the right side. *Center row*: ‘conformal’ plating at lower current density. A center seam is formed. *Bottom row*: ‘Bottom-up’ or ‘Superfill’

(b) Extreme Uniformity Requirements on the Wafer Scale – The thickness uniformity requirements (less than 2-3% variation) across a large, 200 mm wafer exceed any conventional plating specifications. These extreme requirements are imposed in order to minimize the ‘burden’ on CMP, which must remove the excess copper that was plated to assure complete fill. In addition to variations due to substrate and contact resistances, the thickness uniformity is somewhat affected by the electrolyte flow. This poses a difficulty since it is not easy to achieve highly uniform flow across the entire wafer in a fountain-plating configuration. Additionally, the feature density (‘loading’) varies across the wafer, causing variations in the local current densities and in transport, and thereby posing another barrier to thickness uniformity.

(c) Uneven deposit topography across via groups and larger features - Typically, the wafer topography consists of via assemblies surrounded by flat regions with some wide scale (of the order of 10-100 μm) depressions. The plating rate within the vias and trenches, as discussed above, is highly accelerated. In most practical applications, the

vias fill completely within a few (e.g. 10) seconds, whereas the suppressed flat surface including the wider depressions plate very little during that short time. In order to assure complete fill of the wider depressions, (which are often 1 μm deep), additional, much longer deposition time (of the order of minutes) is required. However, the fast growing deposit within the vias, once reaching the surface level does not immediately slow down. This is most likely due to the fact that the fast growing front may contain strongly adsorbed sulfur depolarizers and is free from suppressing additives (e.g. glycols). Redistribution of additives on the newly formed level surface may take time. Consequently, the vias continue their accelerated growth for a while, resulting in a bulge. The situation is particularly severe when a number of vias or trenches are grouped together, leading to a significant ridge that may be double the height of the average surface. By contrast, the deposition rate within the wide depressions is not accelerated, and significant excess deposition ('burden') must be provided before sufficient geometric leveling is achieved. This issue, that places extreme demands on the CMP process, has not yet been satisfactorily resolved.

(d) Contact resistance issues - The contact resistance must be limited to only a few $\text{m}\Omega$ [6], otherwise catastrophic failure due to copper (seed) dissolution (rather than deposition) along the contact circumference occurs. Due to scarcity of wafer area, only small footprint is allowed for the contacts, increasing the local current density and the commensurate voltage drop. This small area and the need for providing a path for electrolyte flow path in the same region, pose serious challenge for the contact designer. Furthermore, since the contact itself may plate, it must be either completely shielded from the electrolyte or a process must be provided for its periodic deplating.

(e) Seed resistance effect ('Terminal effect') - The thin seed layer introduces the so-called 'terminal effect', which leads to thicker deposit near the wafer circumference due the ohmic resistance in the substrate. This issue is further analyzed below.

(f) Seed layer in aggressive geometries - The seed layer is generated by PVD, which essentially is a line of sight process. Consequently, the seed layer within aggressive geometries (narrow, high aspect ratio, perpendicular or backward sloping sidewalls) is often extremely thin, occasionally reaching only a few angstroms in thickness, particularly towards the bottoms of the sidewalls. Such a thin seed may become discontinuous due to copper agglomeration leading to subsequent gap-fill failure. Advances in PVD technology have recently addressed, at least partially, this limitation. However, future reduction in via dimensions may require an alternate seeding process e.g. electroless plating, CVD or perhaps some modification of PVD.

(g) Copper recrystallization - The plated copper surface is continuously undergoing a recrystallization or coarsening process in which the relatively small plated copper grains ($\sim 0.1 \mu\text{m}$) grow to about 1 μm over a period of a few days at room temperature [7]. Generally, larger grain size is preferable, because it provides higher conductivity and minimizes electromigration. Once the wafer is subject to CMP, recrystallization stops. Since it is desirable that all wafers have about the same crystallinity, it may be advisable to subject all plated wafers to accelerated annealing prior to CMP.

COPPER THICKNESS DISTRIBUTION

Scaling Issues

The deposit thickness distribution on the plated wafer spans a broad range of scales (5-6 orders of magnitude); hence the macroscopic and microscopic regimes must be separately analyzed. This is particularly important since the design objectives are quite different on the wafer scale (cm), where extreme uniformity is specified, and the feature scale (μ) where a bottom-up fill (i.e., highly non-conformal distribution) is required. The fact that the two vastly different scales are dominated by different parameters enables the implementation of the process. As discussed below, the distribution on the wafer scale is controlled primarily by the plating cell configuration, the conductivities of the electrolyte and the substrate, the current density, and to a lesser extent by the electrolyte flow. The distribution on the feature scale, on the other hand, is dominated by kinetics and diffusion.

Wafer-Scale (Macroscopic) Current Distribution

The current density (and deposit thickness) distribution on the wafer scale, in the absence of a significant substrate resistance, is characterized in terms of the Wagner number. This dimensionless parameter represents the ratio of the activation resistance (R_a), of the electrode reaction, which typically enhances uniformity, to the ohmic resistance of the electrolyte (R_Ω). The latter is geometry dependent and usually causes non-uniformities.

$$Wa = \frac{R_a}{R_\Omega} = \frac{\kappa}{l} \left(\frac{\partial \eta_a}{\partial i} \right) \sim \frac{\kappa b}{li} \quad [3]$$

Here, κ is the electrolyte conductivity; l is the characteristic length (wafer scale) and $\partial \eta_a / \partial i$ is the slope of the polarization (i vs. V) curve for the deposition reaction. The latter is controlled by the additives composition. The approximation on the right of Eq. 3 pertains to the ‘Tafel regime’ where most copper deposition takes place. Here, b is the ‘Tafel slope’ ($= RT/\alpha F$) of the polarization curve. For uniform distribution, a high Wagner number is desired, corresponding to high electrolyte conductivity, low current density, and a high slope of the polarization curve.

Appropriate cell design, including the application of current shields, can compensate for current density non-uniformities even when the Wa number is low. To increase the electrode polarization, leveling additives are often incorporated in the electrolyte. Since the additives are present in minute amounts, their distribution across the wafer may be flow-dependent.

The Microscopic (Feature-Scale) Current Distribution

The characteristic distance on the feature scale is of the order of a micron, many orders of magnitude smaller than that of the wafer. As a consequence, the controlling mechanism for the current distribution shifts from potential field to mass transport control [8]. The length scale at which mass transport limitations become more significant than the ohmic resistance is given by [8]:

$$l_{crit} < \frac{\kappa RT}{nF i_L (1 - \frac{i}{i_L})} \quad (\text{for mass transport control}) \quad [4]$$

Applying conditions typical to copper plating, we find that the critical length (below which mass transfer becomes dominant) is between about 6 to 600 μm (depending on the process conditions). Accordingly, the current distribution within the micron-scale features is influenced by mass transport with negligible electric field influence.

It should be emphasized that the forgoing analysis compares only the relative importance of mass transport to electric migration. Kinetics resistance, which is not scale-dependent, will typically be the overall dominant resistance in small scales, prevailing over both the mass transport and the ohmic resistances.

Based on this analysis, it is not meaningful to characterize the microscopic current distribution in terms of the Wa number (since the latter is based on the ohmic resistance, whereas on the micro-scale, the concentration field is more important). Instead, the micro-leveling parameter, L , has been formulated [8], replacing (as the source for non-uniform flux) the ohmic resistance by mass transfer resistance and comparing it to the kinetic resistance:

$$L = \frac{R_a^*}{R_c^*} = \frac{|\partial \eta_a / \partial i|}{|\partial \eta_c / \partial i|} = \frac{n i_L \left(1 - \frac{i}{i_L}\right)}{\alpha i} \quad [5]$$

A large value of L ($L \gg 1$) implies, therefore, kinetics resistance dominance. Typically, this is synonymous with uniform current distribution on the micro-scale. If, however, additives adsorption, which controls the deposition kinetics (and the leveling parameter), is *not uniform*, as the case with bottom-up fill is, a high value of L does not warrant uniformity. It assures, however, that the additives distribution will strongly influence the growth rate and deposit distribution, as intended in bottom-up fill.

Controlling the Deposit Thickness Distribution

Since the current distribution on the macroscopic and microscopic scales is dominated by different mechanisms, different means must be applied to control it.

On the wafer (macro-) scale:

- Uniformity can be provided through hardware design, cell shape, shields, etc.
- Resistive substrate effects may be mitigated by using low conductivity electrolyte.
- Flow field for uniform additives and copper transport should be incorporated.

On the micro (feature) scale:

- High transport rate can be provided by high concentrations and sufficient flow.
- ‘Bottom up’ fill can be achieved through proper selection of additive and control of their distribution.

It should be recognized that the cell configuration does not affect the deposit thickness distribution on the via scale. The latter is entirely controlled by the electrolyte composition (including the additives), process conditions, and the local geometry.

RESISTIVE SUBSTRATE ('TERMINAL') EFFECT

The plating current is initially fed from the wafer circumference through the seed layer, which due to its thinness (500 –2000Å) is highly resistive. As a consequence, the current tends to concentrate near the wafer circumference as shown in Fig. 7. As the deposition proceeds, the resistive substrate effect diminishes due to the build-up of a conductive layer. The final deposit profile exhibits, however, the effects of the initial non-uniform deposition.

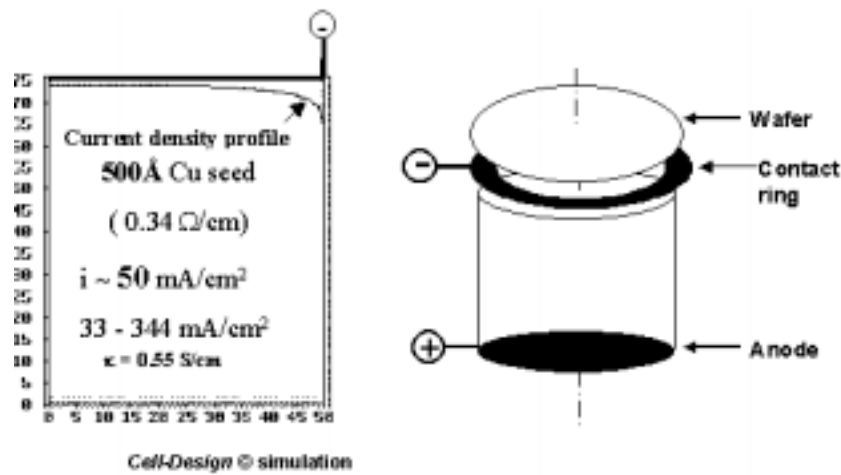


Fig. 7: Schematic of a wafer-plating cell depicting the current feed contact ring (right), and a numerical simulation [9] of the initial current distribution (left), indicating about a 10:1 initial current density ratio between edge (344 mA/cm²) to center (33 mA/cm²) under the simulated conditions (acidified copper sulfate electrolyte).

The effects of resistive substrates on the current distribution ('terminal effect') have been analyzed in the literature [10,11]. Analytical and numerical solutions have been presented for a number of configurations. The non-uniform distribution stems from the current minimizing its passage through the resistive seed layer, and creating a 'shortcut' through the electrolyte towards the contact. Fig. 8 presents a simplistic model based on an equivalent circuit, illustrating (qualitatively) the effect of various parameters. A voltage balance for parallel current paths (Fig. 8-right) through the center of the cell (I_{ctr}) and close to its circumference (I_{edge}) yields:

$$\frac{I_{edge}}{I_{center}} = 1 + \frac{I_{seed}}{I_{center}} \frac{R_{seed}}{R_{electrolyte}} \quad [6]$$

As expected, the current near the edge is larger than that at the center due to the terminal effect. In order to minimize this variation, the seed resistivity, R_{seed} , must be minimized (requiring a thicker seed) or the electrolyte resistance should be increased. This latter approach has been suggested [12].

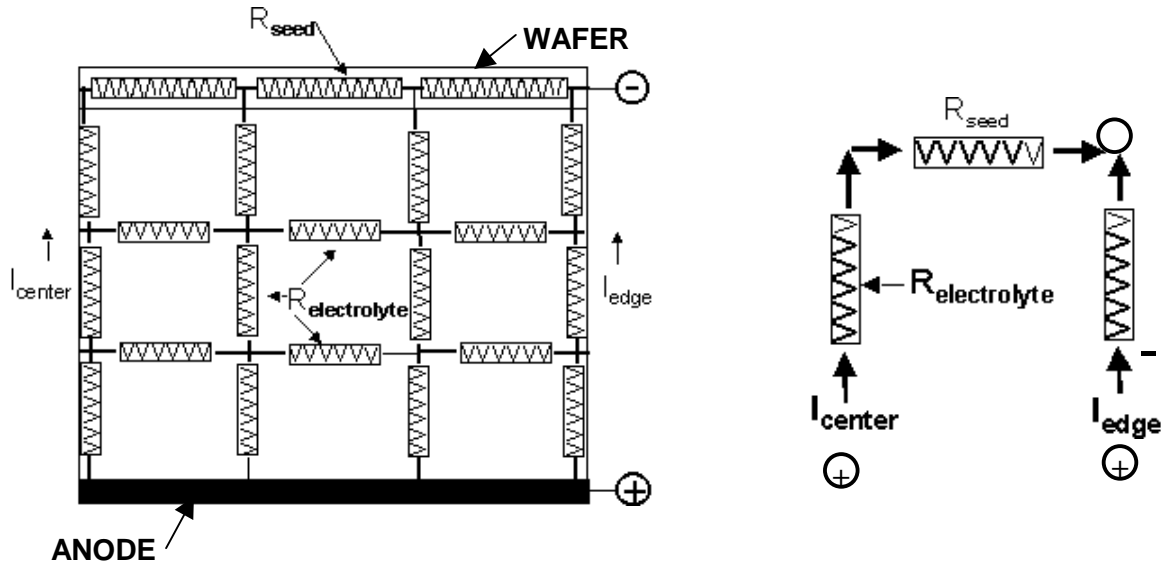


Fig 8: Schematic equivalent resistor network representation of the resistive substrate effect in wafer plating (left), and a reduced ‘minimal’ equivalent circuit (right).

RATIONALE FOR A LOW-ACIDITY ELECTROLYTE

In order to minimize the resistive substrate effect, the use of a *low conductivity* electrolyte is particularly beneficial. Since the proton mobility (introduced via the sulfuric acid) is about 7 times higher than that of copper or sulfate ions, the most effective means of reducing the conductivity is by lowering the acid concentration, or its complete elimination, as suggested by Landau et. al. [12]. Accordingly, the conductivity of a typical copper sulfate electrolyte in the absence of sulfuric acid drops by about a factor of 10, from 0.5 S/cm (in typical copper sulfate with ~1-2 M sulfuric acid) to about 0.05 S/cm (no acid).

The effect of lowering the bath conductivity on the deposit thickness distribution is demonstrated through computer simulations (Fig. 9), using a commercially available software package (Cell-Design[©]) [9]. Cell-Design[©] employs a finite element technique coupled with moving boundaries and a time stepping procedure to simulate deposit growth. A perfect cylindrical cell configuration is modeled; hence all the thickness non-uniformity is due to the resistive substrate. As noted, most of the thickness variation occurs at the initial stages of the deposition process when the substrate resistance is highest. Clearly, removing (or lowering) the acid significantly improves the copper thickness uniformity, which in turn leads to better process integration with subsequent CMP steps.

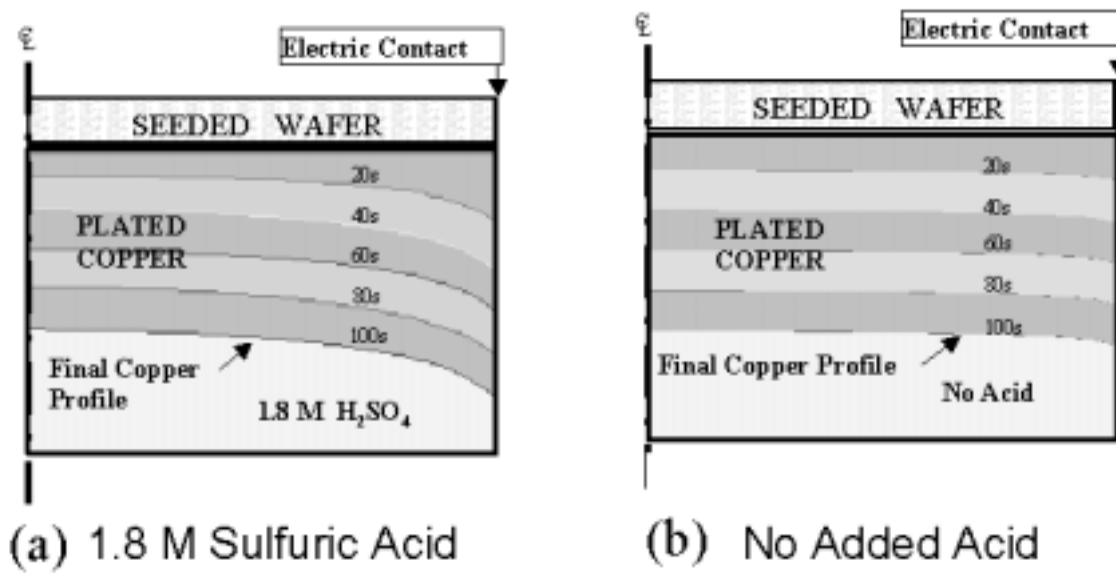


Fig. 9: Computer simulation (Cell-Design[®]) of copper deposition on a resistive wafer. An axisymmetric cross-section through a 200 mm wafer is shown, with the wafer center on the left and the electrical contact on the right. Current density $\sim 35 \text{ mA/cm}^2$. Five growth steps, 20 sec. each, are simulated. The darker region is proportional to the deposit thickness (for clarity, the vertical axis has been magnified). Copper kinetics (no additives) are assumed: $i_0 = 1 \text{ mA/cm}^2$; $\alpha_c = 0.5$; $\alpha_A = 1.5$; $T = 25^\circ\text{C}$. Initial seed thickness is 1000Å. Substrate resistivity is updated with deposit build-up. **(Left):** 0.24 M $\text{CuSO}_4 + 1.8 \text{ M H}_2\text{SO}_4$. Final deposit thickness range: 1.08 – 1.52 μ . (34% variation). **(Right):** 0.85 M CuSO_4 . Final deposit thickness range: 1.28 – 1.41 μ . (9.6% variation).

MASS TRANSPORT CONSIDERATIONS

Unlike the current distribution on the wafer scale, which is typically controlled by the electric field, the current distribution on the micro- (or via-) scale is dominated by kinetics and mass transport. Since the plating additives are present in minute quantities (ppm range), their flux is always transport limited. Because flow is absent within the blind vias, the copper and the additives are transported there solely by diffusion. Copper depletion at the bottom of the vias due to transport limitations will adversely affect the deposit properties.

Since higher flow provides only partial transport enhancement (external to the vias), other means should be applied to enhance copper transport. Minimizing the electrolyte acidity that has been discussed in the context of minimizing the resistive seed effect has a second beneficial effect. The sulfuric acid, when present at high or moderate concentrations, carries most of the current within the electrolyte bulk. Its removal shifts the transport number of the copper ion from about zero to 0.5, thus effectively doubling the copper transport rate. This ‘chemically induced’ transport enhancement [12] is particularly effective for providing adequate copper transport within the blind vias.

Additional enhancement of copper transport can be realized by increasing its bulk concentration (C_B). Copper concentration in conventional plating electrolytes is typically in the range of 0.1 – 0.5 M. Usually, this is sufficient, since transport to large features can be enhanced by flow. In plating micron-scale features, transport enhancement by flow is only partially effective, and a higher copper concentration is sought in order to enhance diffusion into the blind vias. It is difficult to maintain a high copper concentration in a highly acidic electrolyte due to the common ion effect: sulfate ions originating from the sulfuric acid, limit the degree of copper dissociation. Hsueh and Newman [13] compiled copper solubility data showing that in 2M sulfuric acid, the maximal copper solubility is about 0.75 M. In 4 M sulfuric acid, the copper solubility drops to about 0.5 M. One method of supporting a higher copper solubility is switching to an acid that is not sulfate based. Another approach to support higher copper concentration is removing or reducing the sulfuric acid concentration [12]. Accordingly, by minimizing the sulfuric acid (to about pH=2), copper solubility of close to 1.4 M can be reached, and a plating solution with a copper concentration in the range of 0.8 – 1.2 M can be easily maintained.

ELECTROLYTE COMPOSITION

The plating electrolyte consists of major species (molar concentrations) and of minor species (additives in ppm concentrations).

Major Components

The copper-plating electrolyte is based on copper sulfate acidified with sulfuric acid. Although numerous other copper plating electrolytes are available, acidic copper sulfate is by far the most common, and is exclusively used in interconnect metallization. It is very stable, inexpensive, non-toxic, and readily available. The role of the copper sulfate is to provide the copper ion for plating. Early wafer metallization applications used concentrations identical to those in printed circuit plating, i.e., about 0.2-0.6 M. The recognition that the copper deposition within the narrow vias is almost entirely dependent on diffusion, and that higher copper concentration reduces the dependence on flow [12] led to a recent shift in industry towards more concentrated electrolytes, in the range of 0.6 – 1.0 M.

The major role of the sulfuric acid is to provide conductivity to the electrolyte, thereby assuring a uniform macroscopic current distribution (corresponding to a large value of the Wa number). This is essential in conventional plating where a dedicated and specifically designed plating cell is typically not available. As discussed above, this requirement does not apply to wafer metallization where dedicated cells are carefully designed to produce uniform current distribution. On the contrary, here, a more resistive electrolyte that mitigates the effect of the resistive seed is expected to produce a more uniform current distribution. The lower acidity electrolyte offers many other important advantages:

- Less corrosive to the thin seed layer
- Enables higher copper solubility by minimizing the common ion (sulfate) effect

- Provides ‘chemical’ transport enhancement by modifying the copper transport number from zero to 1.
- ‘Greener’ process – Bypass regulatory restrictions on acids, increased environmental acceptance, enhanced operator safety and convenience in handling
- Less corrosive media preserves equipment

The following Table summarizes the information concerning the major electrolyte components. The down-pointing arrows indicate recent trends.

Species	Function	Polarization Effect	Concentration	
			Wafer plating	Conventional
Copper Sulfate	Reactant	Mild accelerator	0.2 - 0.6 M ↓ 0.5 - 1.0 M	0.25 M 0.2 - 0.6 M
Sulfuric acid	Conductivity (Supporting electrolyte)	Mild inhibitor	0.5 - 2 M (pH = 0) ↓ 0.0003 – 0.1 M (pH = 1 - 3.5)	1.8 M 0.5-2 M (pH = 0)

Minor Species (‘Additives’)

Plating electrolytes traditionally contain additives whose function is to modify and control the properties of the plated material and its distribution on the macro- and micro-scales. Typically, plating additives are surface-active compounds that adsorb preferentially on the plated layer. The mechanism by which those compounds affect the plating process is often poorly understood, however, their effects are quite noticeable. Major effects include modifying the appearance of the deposit (color, luster, roughness) and the reaction kinetics. The latter are noted by changes in the polarization curve: typically providing higher slope of the overpotential vs. the current density, thereby affecting also the deposit distribution [14]. Other additives tend to incorporate within the deposit and modify its mechanical or chemical properties (e.g., grain refiners), or change the wetting properties of the interface. Quite often the additives effects are synergistic (i.e. their effects are enhanced in combination). Infrequently, probably due to competitive adsorption, additives negate each other’s effect.

The different copper plating additives are often referred to in terms of functionally descriptive name e.g., carrier, additive, brightener, leveler, grain refiner, etc. However, with the exception of the polyethers, that are commonly named ‘carriers’, all other

names are not uniformly applied. Furthermore, the use of the functionally descriptive terms is simplistic since the effects of the additives are often synergistic. As an example, *either* the chloride ion, the polyether ('carrier') or the organic sulfur compound tend to change (to various degrees) the copper deposit color from light brown when plated without any additives to a bright pink. When applied in *combination*, the deposited copper is lustrous golden yellow.

The following table summarizes the classes of plating additives that are commonly used in copper interconnect metallization. The nitrogen-containing compound (typically quaternary nitrogen) is not uniformly applied and hence some electrolytes contain three (rather than four) additives. On the other hand, some electrolytes contain additional species (that commonly belong to the same or similar groups as listed below). Often, the chloride ion, although present in minute quantities (<100ppm), is not considered an additive and is listed among the major bath constituents.

Species	Name	Function	Polarization	Concentration
Chloride ion		brightens deposit color	Mild inhibitor	40 – 100 ppm
Polyether (PAG polymer) (Polyalkylene-glycol)	Carrier (wetting agent, leveler)	Levels (macroscopic scale) by Monolayer Film Adsorption	Inhibitor (Suppressor)	PAG: 50 – 500 ppm
Organic Sulfide	Additive Brightner	Micro-leveler Grain refiner	accelerator	SPS: 5 -100 ppm
Nitrogen compound	Leveler Dye Surfactant	Micro-leveler Grain refiner Brightner	Strong inhibitor	0 – 20 ppm

The exact function and mechanistic role of the different additives is not completely understood, although numerous observations provide insight. It has been shown that the chloride ion adsorbs at crystal and grain boundaries and affects the copper morphology. Some claim that the chloride stabilizes the Cu^{+1} (cuprous) ion that most likely serves as an intermediate in the copper deposition process. Another role that has been assigned to the chloride ion is to aid in the polyether adsorption on the surface. The only statement that can be made with certainty about the chloride is that it significantly improves the appearance of the deposit and that all major commercial copper plating formulations contain it. As shown in Fig. 10, the chloride acts as a mild inhibitor. Interestingly, if the chloride is present in concentrations larger than about 100 ppm or lower than about 30 ppm its function degrades significantly.

The 'carrier' is a polyether, often in the form of polyethylene or polyalkylene glycol with molecular weight between 500 and 7000. It appears to cover the surface as a

continuous film and provides, as a major function, leveling of the deposit. When excess amount is present and the film thickens at certain locations on the substrate, variable deposit thickness resembling wide steps or terraces is observed. Polarization curves (e.g. Fig. 10) indicate that the polyalkylene glycol is an inhibitor. The glycol plays a major role in the bottom-up fill by inhibiting deposition at the top wafer surface and particularly the rims of the vias. Due to the relatively large size of the molecule, its diffusion rate into the via is probably hindered. No, or minimal amount of the glycol is incorporated in the copper deposit or is decomposed during deposition.

The organic sulfur compound is typically a di-sulfide. A commonly used compound is Bis(3-sulfopropyl)-disodium-sulfonate ($C_6H_{12}Na_2O_6S_4$) which is commercially distributed as 'SPS'. The di-sulfide most likely cleaves at the S-S bond generating two active mono-sulfides that adsorb strongly to copper and serve as micro-levelers. The di-sulfide is often considered a plating accelerator, however, its polarization behavior (e.g., Fig. 10) indicates that the term 'depolarizer' suits better its functionality. By itself, the sulfur additive polarizes the electrode, however, in the presence of e.g. polyalkylene glycols, it appears to reduce the polarization effects of the glycol, perhaps through competitive adsorption. Unlike the glycols, the sulfur additives are consumed in the plating bath, partially through incorporation within the deposit and to a larger extent, through oxidation, primarily at the anode. Too vigorous flow past the anode, a high surface area anode, and excess oxygen in the electrolyte enhance the degradation of the sulfur additive. It seems that the sulfur compound plays a key role in the bottom-up fill. It has been hypothesized that due to its smaller size, the sulfur compound preferentially diffuses into the narrow features, enhancing the bottom-up fill.

The nitrogen containing additives provide high luster to the deposit and serve primarily as grain refiners. These compounds seem to be most effective in the resonant quaternary nitrogen structure that strongly binds to copper and is common to many dyes, although other nitrogen compounds have been effectively used. The amount of added nitrogen varies between about 0.1 to 15 ppm. The nitrogen-based additives are strong suppressors. They do not seem to critically affect the bottom-up fill mechanism and some commercial formulations do not contain the nitrogen-based additives.

Major U.S. chemical suppliers of plating electrolytes for interconnect wafer metallization are Shipley-LeaRonald ('Gleam') and Enthone-OMI ('Cu-bath'). IBM has not disclosed the composition of its proprietary electrolyte, however, it most likely contains similar compounds.

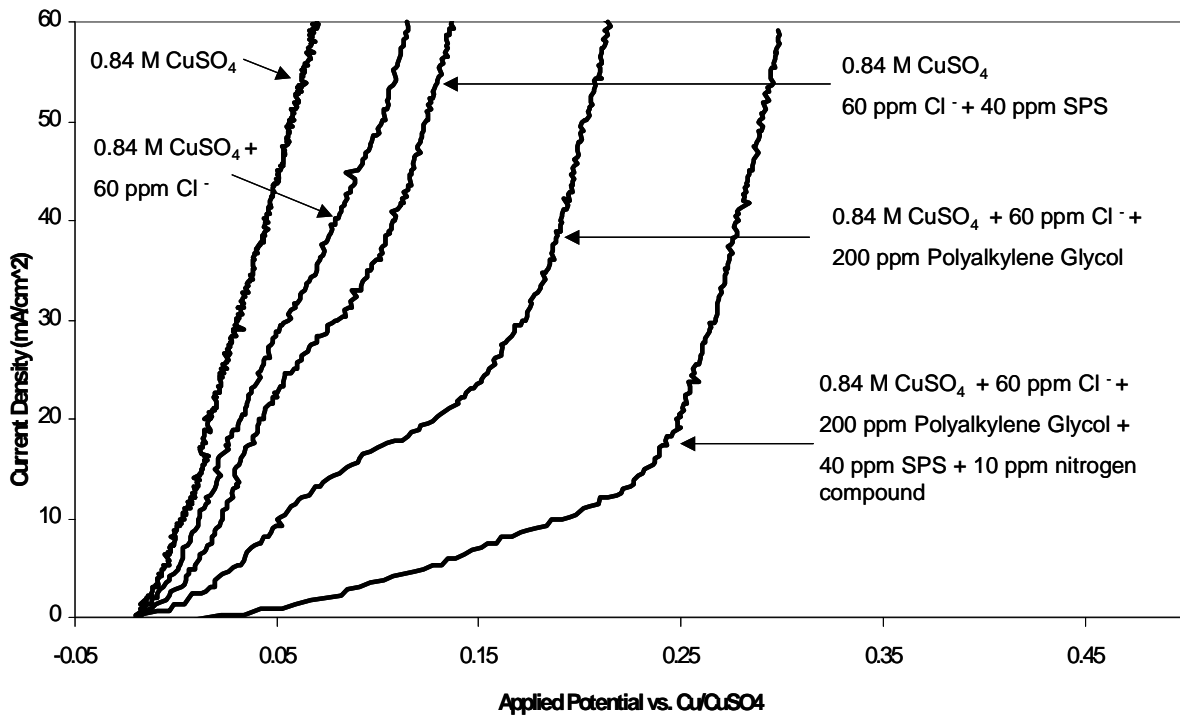


Fig. 10: Polarization curves of typical copper additives combinations. It is noted that all additives bearing systems exhibit higher polarization (inhibition) than the additives-free electrolyte.

CELL AND PROCESS DESIGNS

Cell Configurations

Unlike typical conventional plating cells that are designed to accommodate a variety of parts, copper metallization of interconnects is conducted in a specially designed and *dedicated* tool that is used to plate well-defined disk-shaped silicon wafers. Accordingly the cell configuration and flow pattern may be manipulated to provide the desired uniform macroscopic current distribution across the wafer. The ideal shape that provides a perfectly uniform distribution is a cylindrical cavity with a diameter exactly matching that of the wafer. The wafer must be placed flush against one edge and the anode at the other end, as shown in Fig. 11.

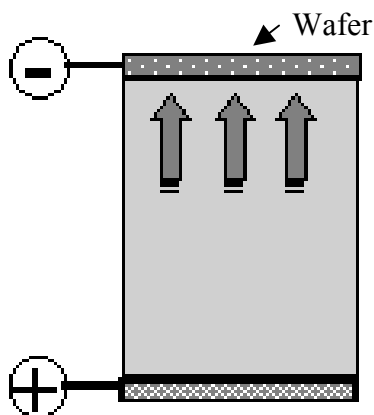


Fig. 11: An ideal cylindrical plating cell characterized by a perfect uniform current distribution on the wafer.

A number of practical considerations interfere with the ideal cylindrical design, as shown schematically in Fig. 12. First, *cavities* must be provided for electrolyte *flow*. These cavities, particularly when present next to the wafer rim, will cause current dispersion and a higher current density near the rim. As a general rule, the larger the cavity, the larger is the region across which the current distribution becomes non-uniform. If the cell diameter is much larger than that of the wafer, or if the wafer is not flush against the cylinder top (which is nearly always the case), current dispersion will occur, leading to excessive edge thickness. These effects may be minimized through the use of properly positioned *shields* and through careful design of the flow cavity next to the wafer edge.

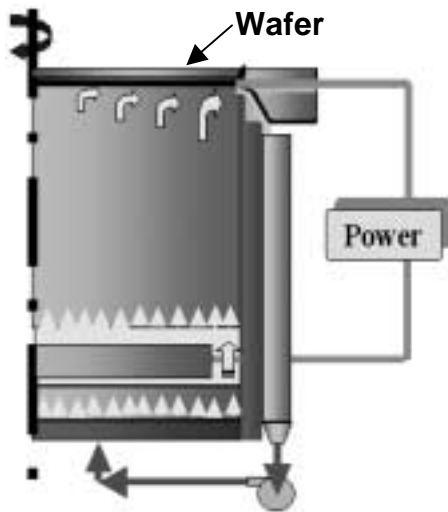


Fig. 12: Schematic of a fountain plating cell configuration. The (rotating) wafer is on top.

A second complication that would cause deviation from the ideally uniform current distribution even if a perfectly bounded cylindrical cell were feasible, is the resistive seed layer effect, as discussed earlier.

Flow Effects

Since the copper plates on the wafer surface far below its limiting current, the effect of flow on the wafer scale distribution is secondary, but not negligible. The copper deposition takes place under kinetics control, and as pointed out [15], in this regime the deposition rate is quite sensitive to the copper concentration at the interface. The copper ion concentration is strongly affected by flow even far from the limiting current. Additionally, the surface additives concentration affects the deposition kinetics, and unless the additive is saturated or controlled by a very slow adsorption process, its surface concentration will be affected by transport [14]. Hence, it is important to generate a uniform flow past the wafer, (unless intentionally non-uniform transport is desired to counter other non-uniformities). Since it is not simple to design, control and maintain a uniform flow field past a relatively large wafer, particularly when the flow

egresses at the wafer circumference, it is perhaps easier to design a process where the flow effect is minimized.

The electrolyte must flow past the anode. Typically, the electrolyte flows through a (cylindrical) gap between the anode circumference and the inner sidewall of the cell. To prevent flow 'short-circuiting' to the exit, and to enhance flow uniformity, a resistive membrane may be placed between the anode and the wafer. To minimize the formation of anode sludge some fraction of the flow can be diverted in a direction parallel to the anode.

Plating Tools Implementations

There are currently three *major* U.S. suppliers of production tools for copper plating on wafers: Applied Materials, Novellus and Semitool. Their detailed cell designs have not been disclosed in the literature, however, based on general descriptions, some similarities and differences can be inferred. All tools are based on a cylindrical fountain configuration where the wafer is immersed, face down, in the electrolyte. All configurations involve wafer rotation, which is relatively slow and is primarily used to even-up the (tangential) uniformity. Electrolyte is circulated towards the wafer in a stagnation (perpendicular) flow.

Applied Material's cell strives to simulate the close-fitting cylindrical configuration as closely as practical. The electrolyte is circulated at a relatively modest rate towards the wafer. Flow uniformity is achieved by circulating it through a relatively tight diaphragm distributor that surrounds the anode compartment and doubles as a filtering medium. Portion of the flow is diverted parallel to the anode and out of the cell. A relatively high copper concentration and lower acidity electrolyte provide, as described earlier, higher copper transport rates and minimize dependence on the flow. The anode is a pure copper cylinder. Discrete contacts feed the current. The inert platinum contacts are partially exposed to the electrolyte and are periodically re-conditioned by anodically stripping the accumulated copper.

Novellus' cell is based on IBM's design and contains a cone-shaped membrane that distributes the flow and possibly also affects the current distribution. The cone diverts portion of the flow past the anode compartment. The anode is phosphorized copper which must be conditioned (to generate an anode film) prior to use. The current is fed through a continuous contact ring, which is kept dry by an elastic seal. Semitool's cell uses a perforated 'distributor' plate that controls the current and perhaps, the flow by its hole pattern. A phosphorized copper anode and discrete contacts are used.

PROSPECTS, CHALLENGES AND OPPORTUNITIES

Although, copper plating of present-day interconnects is production-worthy, a number of important (non-critical) issues remain. These include:

- Improved *thickness uniformity across feature clusters* and scales will reduce the CMP burden. Improvements may be achieved possibly by modifying the plating

conditions to halt the accelerated via cluster growth once it reaches the surface level. More radical solutions may require substantial process modification, which may involve chemistry and/or hardware changes.

- Despite major improvements, the *copper seed layer* is still of marginal thickness in highly aggressive geometries. Future generations of sub 100 nm features may require improvements in seed coverage. CVD or electroless plating are obvious contenders. The latter may also be used for seed ‘repair’. Major issue is adhesion.
- Future introduction of low-k dielectrics is likely to present major integration issues. In particular, *CMP of a brittle low-k material* is difficult. Electropolishing may be used to an advantage; however, its planarization capabilities must first be improved. On the other hand, a variant of low-force CMP which will be largely based on chemical dissolution rather than on abrasion, may be developed.
- Improved, more robust and more accurate *process analysis and controls* are still needed.
- *Fundamental understanding*, a key to process improvements and control, is still lacking in many critical aspects. The detailed mechanism by which the various additives affect the copper deposition, including the bottom-up fill process itself is still lacking.
- *Simulation tools* including computer aided design are needed for scaling and optimization
- Wet *electrochemical processes*, e.g., electroplating, electroless plating, electrodisolution, and electropolishing, being inherently less costly and faster than ‘dry’ processes, are likely to find *additional applications* in semiconductor processing

SUMMARY AND CONCLUSIONS

Copper electroplating of semiconductor interconnects using the dual damascene process offers significant advantages and will replace aluminum in most interconnect applications. The plating process is production ready and has been integrated with commensurate processing steps. The process can be used reliably in aggressive geometries down to feature sizes of about 100 nm. Extending the process to significantly smaller feature sizes (in aggressive geometries) may require improvements, particularly in the seed layer deposition technology. Improvements are likely to follow, particularly in the area of enhancing thickness uniformity across features spanning different scales. Integration with brittle, low-k dielectrics poses challenges particularly to the ECM step. Electropolishing may offer an alternate or complementary processing route for such structures. Although good modeling capabilities of the current distribution exist, enhanced fundamental understanding of the deposition process and particularly, detailed mechanistic understanding of the additives action is needed. Undoubtedly, wet electrochemical processes will find additional applications in semiconductor processing.

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LIST OF SYMBOLS

b	Tafel slope, $RT/\alpha F$, Ω
C	concentration, mole/cm ³
C	capacitance, cb/volt
D	diffusivity, cm ² /sec
F	Faraday's constant, 96487 C/equiv
i	current density, A/cm ²
i_0	exchange current density, A/cm ²
i_L	limiting (diffusion) current, A/cm ²
I	current, A
l	characteristic length, cm
L	micro-leveling parameter, (ratio of activation to mass-transfer resistance)
n	number of electrons transferred in electrode reaction per mole reactant
r	radius, cm
R	universal gas constant, 8.3143 J/mole-deg
R	resistance, ohm
T	absolute temperature, deg K
Wa	Wagner number, (ratio of activation to ohmic resistance), dimensionless
α_a, α_c	transfer coefficients, anodic and cathodic, respectively, dimensionless
δ_c	equivalent mass transfer boundary layer thickness (Nernst-type), cm
η	overpotential, V
κ	conductivity, S/cm
ρ	resistivity, Ω cm
τ	time constant, sec

Subscripts

a	activation (kinetics)
avg	average
B	bulk
c	mass transport
$crit$	critical
Ω	ohmic

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